AN3157
Application note

STEVAL-IPE010V1 poly-phase demonstration kit for the STPMC1 and STPMS1

Introduction

This application note describes the STEVAL-IPE010V1 poly-phase demonstration kit for the STPMC1 and STPMS1.The STPMC1 is a metering ASSP implemented through an advanced 0.35 µm BCD6 technology.

The STPMC1 device functions as an energy calculator in power line systems, using the Rogowski current transformer and shunt or Hall current sensors. It is used in combination with one or more STPMS1 devices. It implements all the functions needed in a 1, 2 or 3-phase energy meter, providing the effective measurement of active and reactive energies, V_{RMS}, I_{RMS}, instantaneous voltage and current-per-phase in 1, 2 or 3-phase wye and delta services, from 2 to 4 wires.

In a stand-alone configuration the STPMC1, which sends a pulse train signal with a frequency proportional to the cumulative active power, can directly drive a stepper motor, therefore implementing a simple active energy meter.

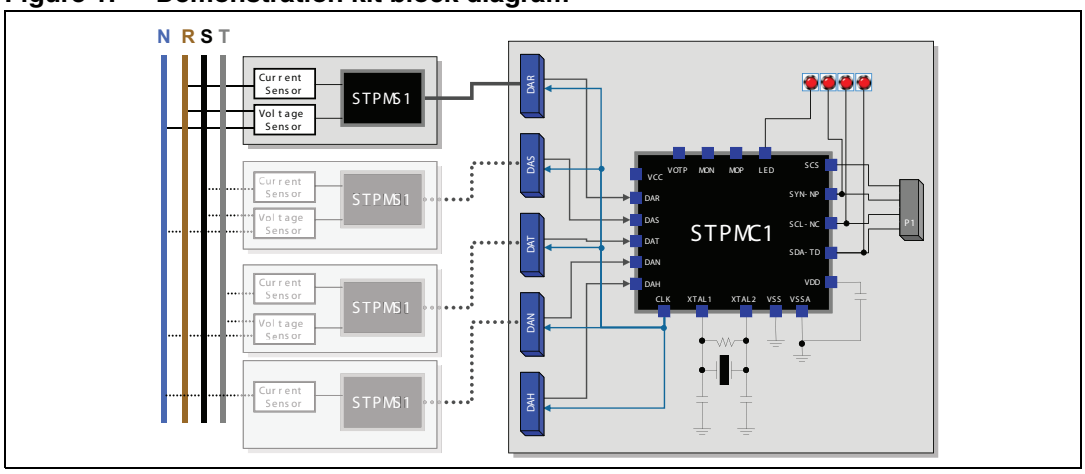
This device can also be coupled to a microprocessor for multi-function energy meters. In this case, the measured data is read at a fixed time interval from the device internal registers by the microcontroller through the SPI interface.

The STPMS1 is an ASSP designed as a building block for single or multi-phase energy meters. It consists of a pre-amplifier and two 1st order ΔΣ modulators, band-gap voltage reference, a low-drop voltage regulator and DC buffers in its analog section, and a clock generator and output multiplexer in its digital section.

The demonstration kit is made up of a main board with the STPMC1 mounted, and it can be coupled with up to 5 daughterboards, each with an STPMS1 mounted to sense the voltage and current of each phase.

Note: The demonstration kit is available on request.

Figure 1. Demonstration kit block diagram



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1 Application description

The purpose of this STEVAL-IPE010V1 demonstration kit is to provide an evaluation platform for the STPMC1 and STPMS1 devices, but it can also be used as a starting point to design a Class 1 meter for 2 to 4-wire power line systems using delta or wye service.

Each phase is monitored by an independent daughterboard, in which an autonomous power supply is provided to the board itself and, once it is connected, also to the motherboard.

In this board, the STPMS1 device senses the phase current through a CT or a shunt sensor, and the phase voltage through a voltage divider. The presence of dedicated networks reduces greatly the sampling (aliasing) noise and the crosstalk noise between voltage and current channels, increasing meter precision. The STPMS1 produces a sigma-delta stream, sent together with the supply voltage, to the STPMC1 through a card edge connector.

The motherboard receives the sigma-delta streams from the daughterboards which are further elaborated by the STPMC1. This device, from a 4.194 MHz crystal oscillator, provides a common clock with programmable frequency to all the daughterboards.

The motherboard, through a 10-pin flat cable connector (P1 in *Figure 2*) can be interfaced to a microprocessor board to implement advanced metering features (multi-tariff, data management and storage, communication, etc). It also has stepper motor connectors for a simple energy meter implementation (W2, W5 in *Figure 2*).

The STPMC1 board can also be connected to a dedicated GUI (graphical user interface) through the STPMxx parallel programmer/reader released with the application.

1.1 Operating conditions

Table 1. Operating conditions

Condition	Value	Unit
V_{NOM}	230	V_{RMS}
I_{NOM}	CT: I_{NOM} = 1 Sh: I_{NOM} = 5	A_{RMS}
I_{MAX}	CT: I_{MAX} = 30 Sh: I_{MAX} = 80	A_{RMS}
f_{LIN}	50 / 60 ± 10%	Hz
T_{OP}	- 40 / + 85	°C

2 Circuit description

2.1 Motherboard circuit

The motherboard consists of the following sections:

- STPMC1 circuit
- Connectors

The schematic of the board is shown in *Figure 2* and in *Figure 3*.

Figure 2. STPMC1 circuit schematics

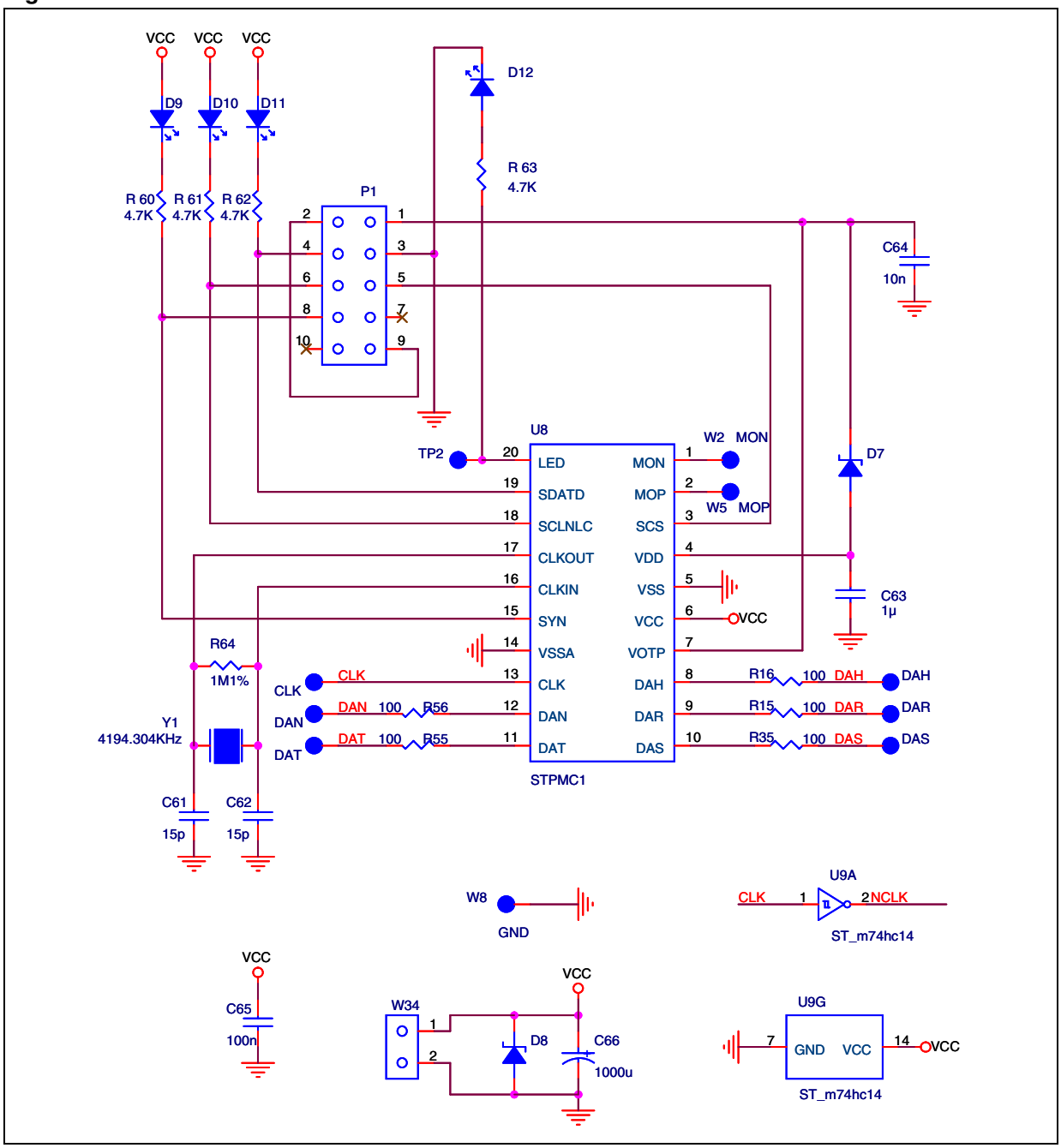
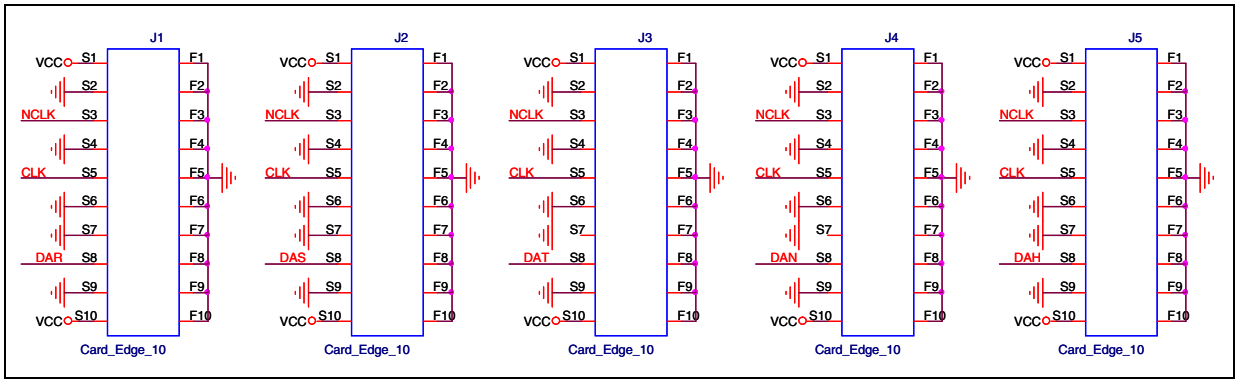


Figure 3. Motherboard connector schematics



2.2 Daughterboard circuit

This section describes the implementation of each phase network which performs the power measurement.

The schematic can be divided into the following subsets:

- Current sensing circuit (1) or (2)
- Anti-aliasing filter (3)
- Voltage sensing circuit (4)
- Crosstalk cancellation network (5)

2.2.1 Current sensing circuit

The STPMS1 has an external current sensing circuit using either a current transformer, in which a burden resistor is used to produce a voltage between CIN and CIP proportional to the current measured, or a shunt resistor.

2.2.2 Anti-aliasing filter

The anti-aliasing filter is a low-pass filter which has a negligible influence on the voltage drop between CIN and CIP, and VIN and VIP. The aim of which is to reduce the distortion caused by the sampling (also called aliasing) by removing the out-of-band frequencies of the input signal before sampling it with the analog-to-digital converter.
Filtering is easily implemented with a resistor-capacitor (RC) single-pole circuit which obtains an attenuation of - 20 dB/dec.

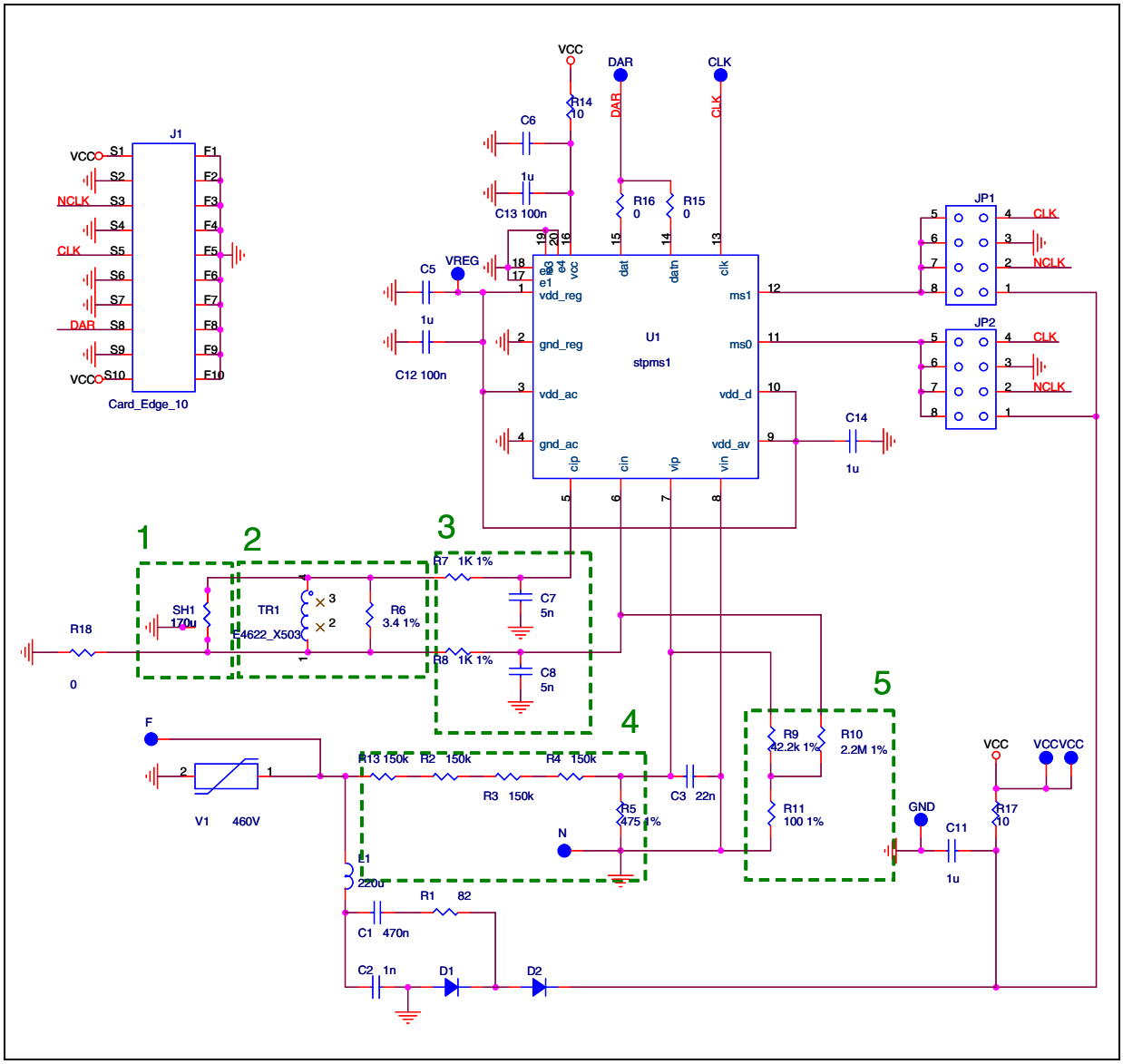
2.2.3 Voltage sensing circuit

A resistor divider is used as a voltage sensor. The 600 kΩ resistor is separated into four, 4 x 150 kΩ, in-series resistors, which ensure that a high voltage transient does not bypass the resistor. This also reduces the potential across the resistors, thereby decreasing the possibility of arcing. The following resistors are used to implement the resistor divider:

- R = R13 + R2 + R3 + R4 = 600 kΩ
- R5 = 475 Ω

The L1 inductor and the C2 capacitor create a filter which prevents electromagnetic interference (EMI).

Figure 4. Daughterboard circuit schematic



2.2.4 Crosstalk cancellation network

The voltage front-end handles voltages of considerable amplitude, which makes it a potential source of noise. Disturbances are readily emitted into current measurement circuitry where they interfere with the actual signal to be measured. Typically, this produces a non-linear error at small signal amplitudes and non-unity power factors. At unity power factors, voltage and current signals are in phase and crosstalk between voltage and current channels merely appears as a gain error, which can be calibrated. When voltage and current are not in phase, crosstalk has a non-linear effect on the measurements, which cannot be calibrated.

Crosstalk is minimized through good PCB planning and the proper use of filter components in the crosstalk network. Recommended filter components are shown in *Figure 4*. The network subtracts a signal proportional to the voltage input from the current input. This prevents crosstalk.

2.2.5 Jumper settings

The on-board jumpers JP1 and JP2 allow the setting of the STPMS1 device according to *Table 2* and *Table 3* below:

Table 2. Modes of operation

JP1	MS0	Description
1	1	Rogowsky mode, ampl = 32
2	NCLK	ampl = 32 (reserved for future expansion)
3	0	Current transformer mode, ampl = 8
4	CLK	shunt mode, ampl = 32, fclk = 8*mclk

Table 3. Changing of band-gap voltage reference

JP2	MS1	Description
1	1	TC = 190 ppm/°C
2	NCLK	TC = 125 ppm/°C
3	0	TC = 100 ppm/°C
4	CLK	TC = 170 ppm/°C

For further details on device configuration please refer to the device datasheet.

2.3 Clock management network

A 4.194 MHz quartz is used to supply the clock for the STPMC1 device. To set this frequency, internal configuration bits MDIV and FR1 must be kept cleared.

A synchronized clock is provided to all STPMS1 devices through the CLK pin, the frequency of which is programmable through bit HSA to 1.049 MHz or 2.097 MHz.

2.4 Communication with microprocessor

A control board with an embedded microprocessor may be connected to connector P1 using a 10-wire flat cable. *Table 4* describes the pinout of the connector.

The STPMC1 has an SPI communication port implemented by four multi-purpose pins (SCS, SYN-NP, SDA-TD, SCL-NLC).

In stand-alone operating mode these multi-purpose pins produce:

- negative power direction on the SYN-NP pin
- tamper condition detected on the SDA-TD pin
- no load condition detected on the SCL-NLC pin

For this reason these pins are connected to the three LEDs D9, D10 and D11.

In this configuration, the LED pin produces a pulse train with a frequency proportional to the 3-phase power and is connected to LED D12.

When configured in peripheral operating mode, the SPI port is enabled and some microcontroller-based applications can either read internal data records or write the mode and configuration signals by means of a dedicated protocol, or reset the device.

By default, the STPMC1 is configured in peripheral mode (configuration bits APL=0).

This also implies the following output settings:

- watchdog reset signal on the MON pin
- zero-crossing (ZCR) on the MOP pin
- programmable energy pulsed output on the LED pin

For further information on STPMC1 programmable bit settings please refer to the device datasheet.

Table 4. P1 connector pin description

Pin	Pin name	Functional description
1	VOTP	Power supply input of +15.0 V during permanent write to OTP cells
2	---	Not connected
3	GND	Signal reference level 0 V and power supply return
4	SDA-TD	SPI interface data
5	SCS	SPI interface enable
6	SCL-NLC	SPI interface clock
7	---	Not connected
8	SYN-NP	SPI interface signal
9	---	Not connected
10	VCC	Power out of +3.3 or 5 V

The P1 connector is also used during the evaluation phase to connect the measurement module to a PC through the STPMxx parallel programmer/reader hardware interface.

This allows the user to set the internal STPMC1 registers temporarily and/or permanently, using a dedicated GUI.

The VOTP pin on the P1 connector is used when a host wants to permanently write some configuration bits in the STPMC1 device. In this case, a +15 V power level must be present on the VOTP. This level must be delivered from the host itself because the module does not have an on-board charge pump.

3 Board layout

3.1 Layout rules for the 3-phase system design

Noise rejection is the main concern when a 3-phase multi-chip approach is chosen. In this case, layout plays a crucial role.

Below are some rules to follow in the layout phase of 3-phase systems:

- Component positioning

The components of the measuring section (STPMS1, current sensor, passive components) should be placed using the same layout for each phase. The phases should be placed in a symmetrical scheme. In this way a reduction in crosstalk can be achieved.

The current sensor should be placed very close to the corresponding STPMS1 to minimize the captured noise.

- Component routing

The passive components belonging to the analogue input channels must be placed between the sensor and the STPMS1, always respecting a symmetrical scheme.

- Quartz

The crystal network must be placed close to the STPMC1, and a completely symmetrical path from the CLK pin of the STPMC1 to the STPMS1 devices must be ensured. A copper plate is placed under the crystal, both on the top and on the bottom side of the PCB.

- Grounding

The STPMS1 device must be grounded by an exposed pad and by the VSS pin ensuring maximum stability of the ground plane by placing vias between the top and bottom ground plane. Analog and digital ground must be separated.

3.2 Motherboard layout

Figure 5. Motherboard top layout

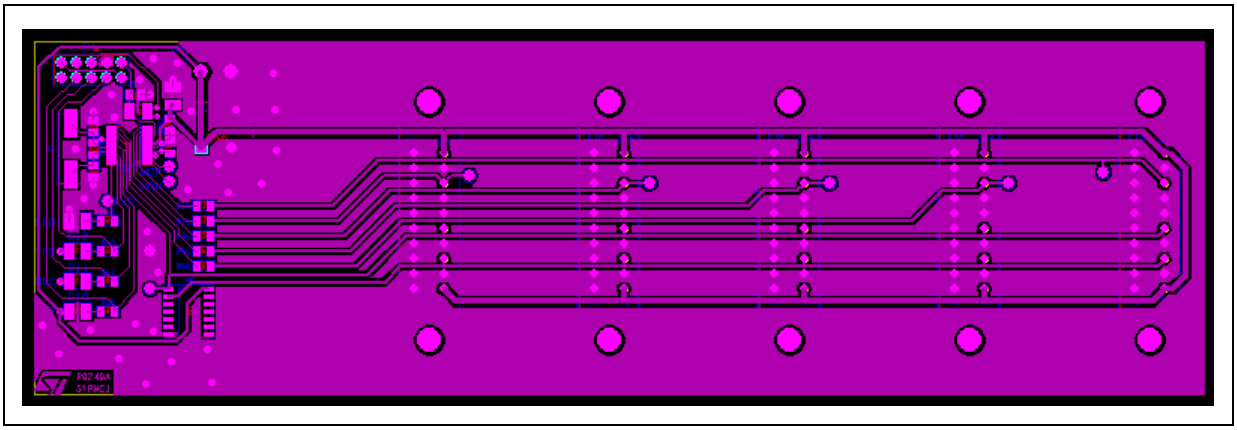
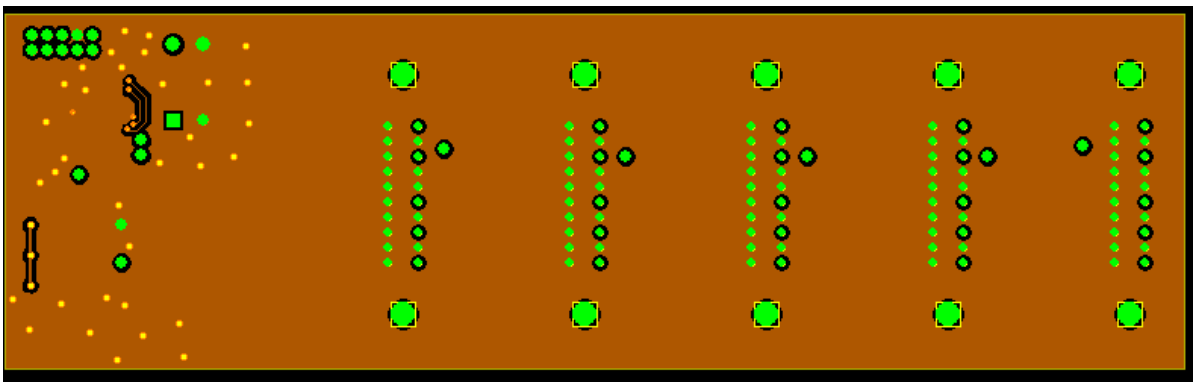


Figure 6. Motherboard bottom layout



3.3 Daughterboard layout

Figure 7. Daughterboard top layout

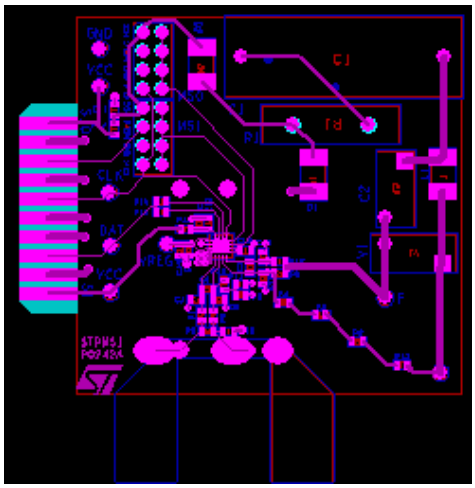
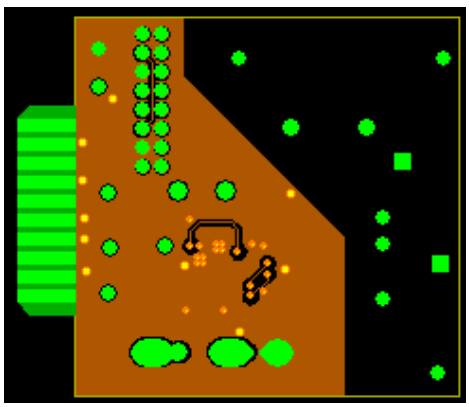


Figure 8. Daughterboard bottom layout



4 Experimental results

The tests have been conducted considering I_{NOM} = 5 A, V_{NOM} = 230 V, f_{line} = 50 Hz.

4.1 3-phase energy measurement accuracy

4.1.1 Test with symmetrical voltages and balanced load at P_F = 1

This 3-phase energy measurement has been carried out in the following conditions:

$V_R = V_S = V_T = 230$ [V_{RMS}]

$I_R = I_S = I_T = I$ [A_{RMS}]

$P_F = 1$

Table 5. 3-phase energy measurement

I (A)	% of In	Error (%)
10	200%	0.013%
8	160%	0.018%
5	100%	0.013%
2	40%	0.112%
1	20%	0.086%
0.5	10%	0.160%
0.2	4%	0.543%

Figure 9. Experimental results graph of the 3-phase energy measurement

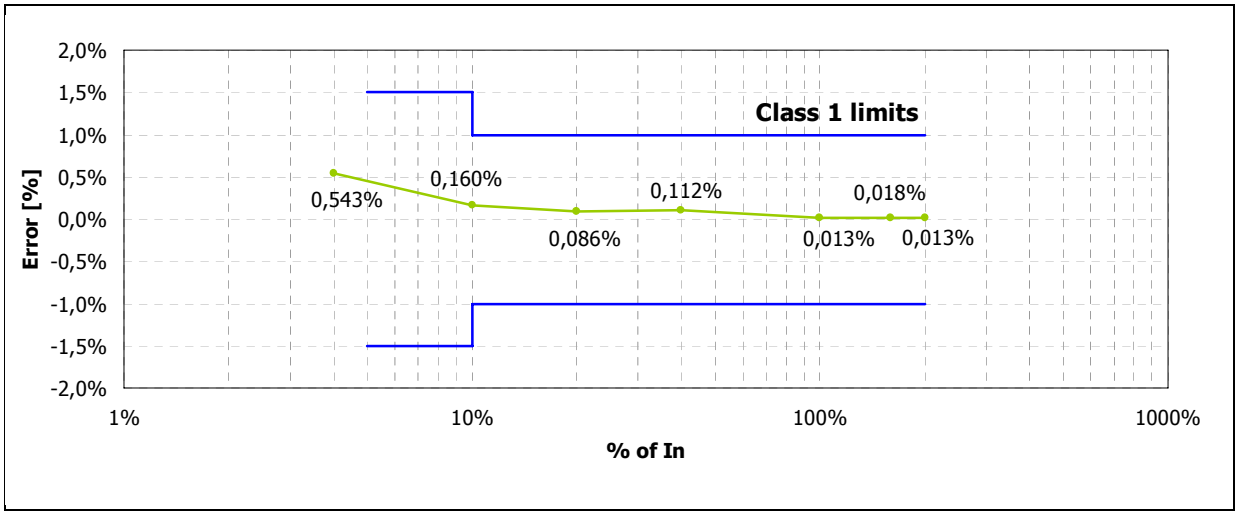


Table 6. Limits for class 1 meters: poly-phase meters with symmetrical voltages and balanced loads at $P_F = 1$

I (A)	% of In	Error (%)
2*In	200%	± 1%
In	100%	± 1%
0.2*In	20%	± 1%
0.1999*In	19.99%	± 1%
0.1*In	10%	± 1%
0.0999*In	9.999%	± 1.5%
0.05*In	5%	± 1.5%

4.2 Typical phase energy measurement accuracy

4.2.1 Test with only one phase load at $P_F = 1$

This single phase energy measurement has been carried out in the following conditions:

$V_R = 230\ [V_{RMS}]$

$I_R = I\ [A_{RMS}]$

$P_F = 1$

Phases S and T not connected.

Table 7. Phase energy measurement

I (A)	% of In	Error (%)
10	200%	0.026%
8	160%	0.034%
5	100%	-0.006%
2	40%	-0.049%
1	20%	-0.069%
0.5	10%	-0.062%
0.2	4%	-0.060%

Figure 10. Experimental results graph of one-phase energy measurement

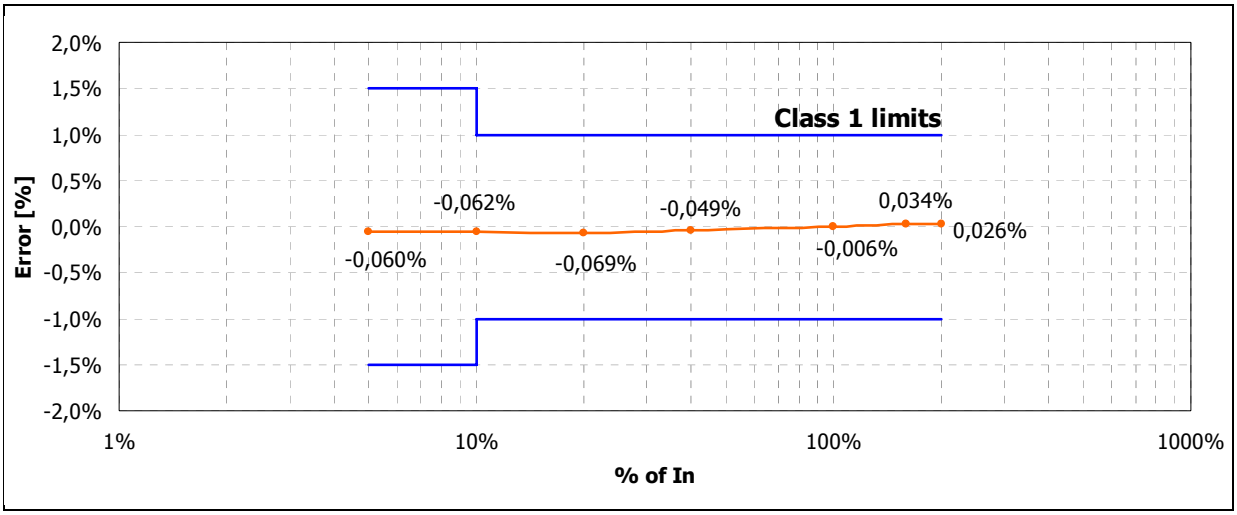


Table 8. Limits for Class 1 meters: single-phase meters at P_F = 1

I (A)	% of In (%)	Error (%)
2*In	200%	± 1%
In	100%	± 1%
0.2*In	20%	± 1%
0.1999*In	19.99%	± 1%
0.1*In	10%	± 1%
0.0999*In	9.999%	± 1.5%
0.05*In	5%	± 1.5%

4.3 Test with only one phase load at P_F = 0.5 inductive and 0.8 capacitive

This single-phase energy measurement has been carried out in the following conditions:

V_R = 230 [V_{RMS}]

I_R = I [A_{RMS}]

Phases S and T not connected

P_F = 0.5 inductive and 0.8 capacitive

Table 9. Phase energy measurement P_F = 0.5 inductive

I (A)	% of In	Error (%)
10	200%	0.031%
8	160%	0.093%
5	100%	0.100%
2	40%	0.053%
1	20%	0.061%
0.5	10%	-0.022%
0.2	4%	-0.300%

Table 10. Phase energy measurement P_F = 0.8 capacitive

I (A)	% of In	Error (%)
10	200%	-0.032%
8	160%	-0.035%
5	100%	-0.041%
2	40%	-0.070%
1	20%	0.051%
0.5	10%	-0.085%
0.2	4%	0.077%

Figure 11. Experimental results graph of one-phase energy measurement

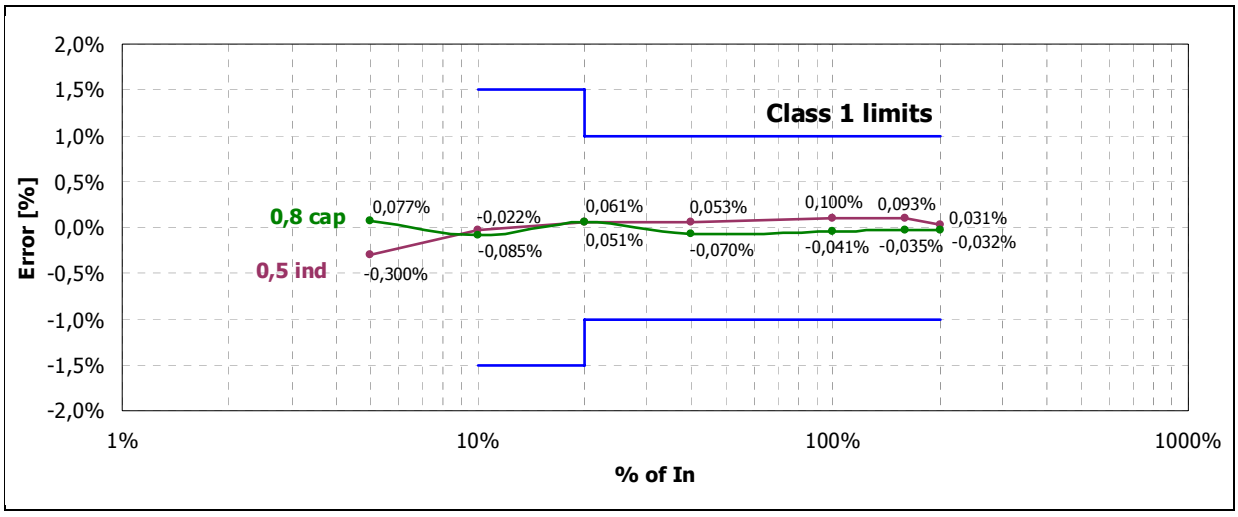


Table 11. Limits for Class 1 meters: single-phase meters at P_F = 0.5 inductive and 0.8 capacitive

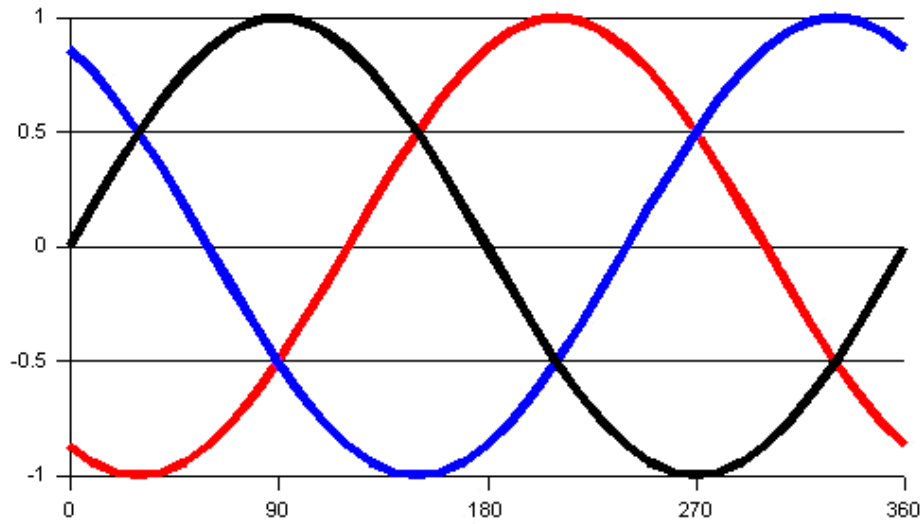
I (A)	% of In (%)	Error (%)
2*In	200%	± 1%
In	100%	± 1%
0.2*In	20%	± 1%
0.1999*In	19.99%	± 1.5%
0.1*In	10%	± 1.5%
0.0999*In	9.999%	
0.05*In	5%	

Appendix A 3-phase systems

3-phase is a common method of electrical power transmission. It is a type of poly-phase system used to power motors and many other devices.

The currents are sinusoidal functions of time, all at the same frequency but with different phases. In a 3-phase system the phases are spaced equally, giving a phase separation of 120°. The frequency is typically 50 Hz in Europe and 60 Hz in the US and Canada.

Figure 12. Instantaneous voltage (or current) in a one-voltage cycle of a 3-phase system



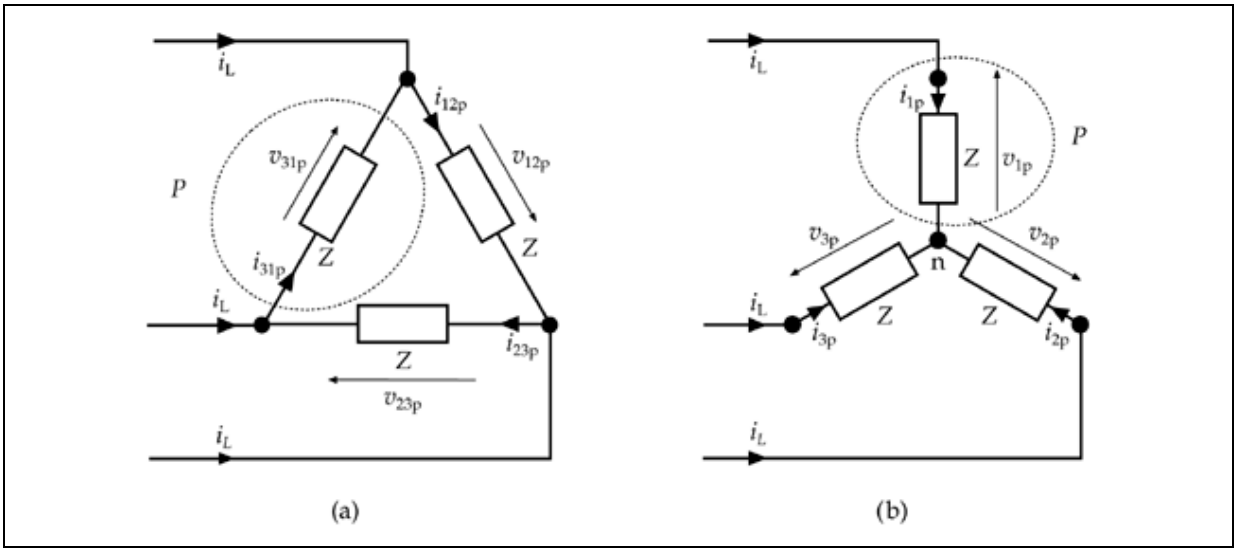
It is possible to supply the three phases over six wires, with two wires reserved for the exclusive use of each phase. However, they are generally supplied over three or four wires:

- Three phases, 3-wire delta service which has no neutral and 220 V between phases.
- Three phases, 4-wire delta and wye service which has 220 V between phase-neutral and 380 V phase-phase.

A.1 Power in 3-phase AC circuits

Let's assume that the angle between the phase voltage and the phase current is θ, which is equal to the angle of the load impedance. Considering the load configurations given in *Figure 13*, the phase power and the total power can be easily estimated.

Figure 13. Per-phase powers in (a) delta-connected load and (b) wye-connected load.



In the case of *Figure 13* (a), the total active power is equal to three times the power of one phase:

Equation 1

$$P_1 = P_2 = P_3 = P = V_{line} I_{phase} \cos\theta$$

Equation 2

$$P_{Total} = 3P = 3V_{line} I_{phase} \cos\theta$$

Since the line current in the balanced delta-connected loads is:

Equation 3

$$I_{line} = \sqrt{3} I_{phase}$$

If *Equation 3* is substituted into *Equation 2*, the total active load becomes:

Equation 4

$$P_{Total} = \sqrt{3} V_{line} I_{line} \cos\theta$$

In *Figure 13* (b), however, the impedances contain the line currents I_{line} (equal to the phase current, I_{phase}) and the phase voltages:

Equation 5

$$V_{phase} = V_{line} / \sqrt{3}$$

Therefore, the phase active power and the total active power are:

Equation 6

$$P_1 = P_2 = P_3 = P = V_{phase} I_{line} \cos\theta$$

Equation 7

$$P_{Total} = 3P = 3V_{phase} I_{line} \cos\theta$$

If the relationship between the phase voltage and the line voltage is used, the total active power becomes identical to *Equation 4*. This means that the total power in any balanced 3-phase load (Δ or Y-connected) is given by *Equation 4*.

Similarly, the total reactive and the total apparent power in the 3-phase balanced AC circuits can be given by:

Equation 8

$$Q_{Total} = \sqrt{3} V_{line} I_{line} \sin\theta$$

Equation 9

$$S_{Total} = \sqrt{3} V_{line} I_{line}$$

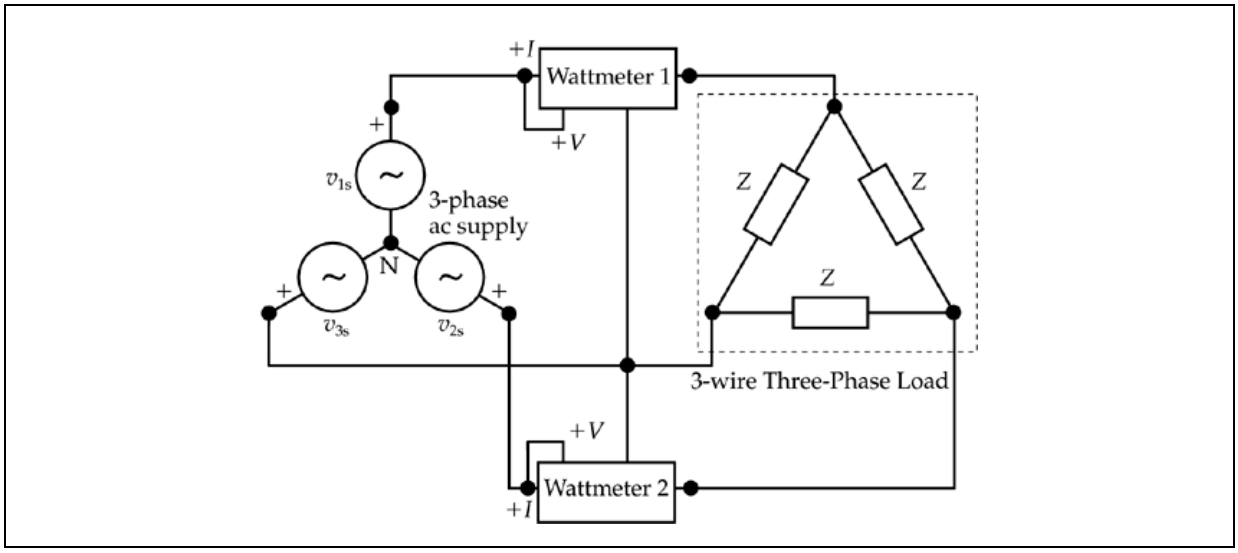
A.2 Power measurement techniques

In 3-phase power systems, one, two, or three wattmeters can be used to measure the total power. A wattmeter may be considered to be a voltmeter and an ammeter combined in the same box, which has a deflection proportional to $V_{rms} I_{rms} \cos\phi$, where ϕ is the angle between the voltage and current. Therefore, a wattmeter has two voltage and two current terminals, which have + or - polarity signs. Three power measurement methods utilizing the wattmeters are described next, and are applied to the balanced 3-phase AC load.

A.2.1 Two-wattmeter method

This method can be used in a 3-phase three-wire balanced or unbalanced load system that may be connected to Δ or Y. To perform the measurement, two wattmeters are connected as shown in *Figure 14*.

Figure 14. The two-wattmeter method in star- or delta-connected load.



In the balanced loads, the sum of the two wattmeter readings gives the total power. This can be proven in a star-connected load mathematically using the power reading of each meter as:

Equation 10

$$P_1 = V_{12}I_1\cos(30° + \theta) = V_{line}I_{line}\cos(30° + \theta)$$

Equation 11

$$P_2 = V_{32}I_3\cos(30° - \theta) = V_{line}I_{line}\cos(30° - \theta)$$

Equation 12

$$P_{Total} = P_1 + P_2 = \sqrt{3}V_{line}I_{line}\cos\theta$$

The difference between the readings is computed as follows:

Equation 13

$$P_2 - P_1 = V_{line}I_{line}\cos(30° - \theta) - V_{line}I_{line}\cos(30° + \theta) = V_{line}I_{line}\sin\theta$$

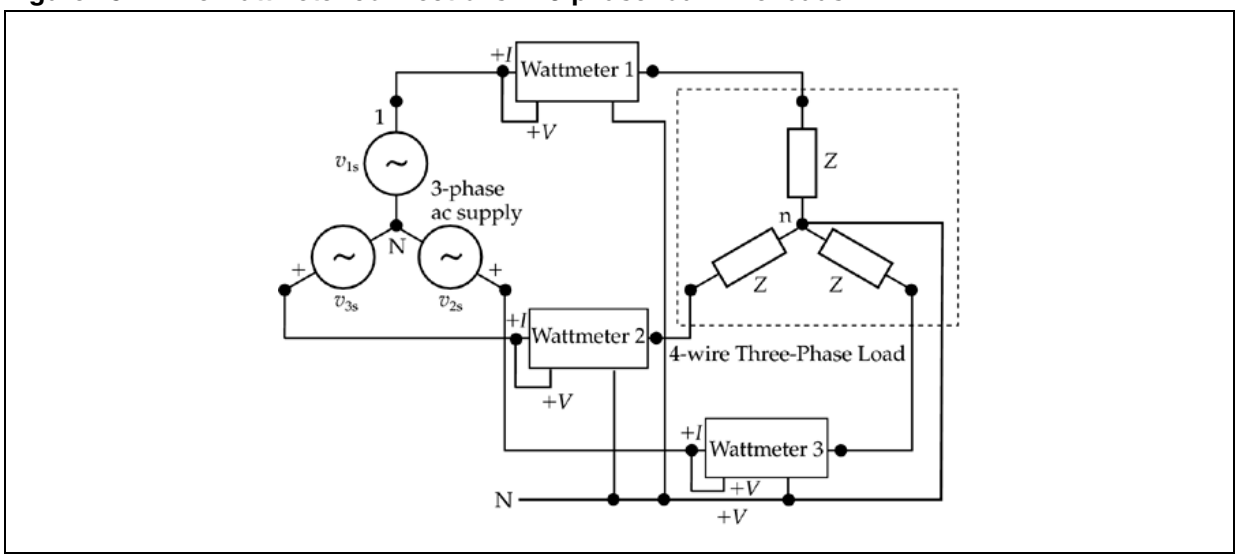
which is $1/\sqrt{3}$ times the total 3-phase reactive power (see *Equation 8*). This means that the two-wattmeter method can also indicate the total reactive power in the 3-phase loads and also the power factor.

A.2.2 Three-wattmeter method

This method is used in a 3-phase four-wire balanced or unbalanced load. The connections are made with one meter in each line as shown in *Figure 15*. In this configuration, the total active power supplied to the load is equal to the sum of the three wattmeter readings.

$$P_{Total} = P_1 + P_2 + P_3$$

Figure 15. The wattmeter connections in 3-phase four-wire loads



A.2.3 One wattmeter method

This method is suitable only in 3-phase four-wire balanced loads. The connection of the wattmeter is similar to the drawing in *Figure 15*. The total power is equal to three times the reading of only one wattmeter which is connected between one phase and neutral.

Appendix B BOM list

Table 12. Motherboard BOM list

Item	Quantity	Reference	Part	PCB footprint	Description
1	2	C61,C62	15p	sm_0805	
2	1	C63	1u	sm_0805	
3	1	C64	10n	sm_0805	
4	1	C65	100n	sm_0805	
5	1	C66	1000u	cpcyl1_d500_ls200_040	Capacitor AL-RILL 13x22/2M*1000my 25V
6	2	D7	Diode	sm_d_1206	Diode planar 1N4148 SOD323*75V
6	2	D8	Diode_zener	sm_d_1206	Diode Zener ZMM SOD 80*5.1V (3.3V) G
7	4	D9,D10,D11,D12	Diode_led	plcc2	SMD LED low current super-red P-LCC-2 OSRAM (Distrelec 631039)
8	5	J1,J2,J3,J4,J5	Card_Edge_10	sullins_10_drxi	
9	1	P1	Connector_5x2	jumper_5x2_bis	
10	5	R15,R16,R35,R55,R56	100	sm_0805	
11	4	R60,R61,R62,R63	4.7k	sm_0805	
12	1	R64	1M1%	sm_0805	
13	1	TP2	TP	TEST_POINT	
14	1	U8	STPMC1	sog_65m_20_w300_l260	
15	1	U9	ST_M74HC14	sog_050_14_w325_l350	
16	1	W2	MON	TEST_POINT	
17	1	W3	DAH	TEST_POINT	
18	1	W4	DAR	TEST_POINT	
19	1	W5	MOP	TEST_POINT	
20	1	W6	DAS	TEST_POINT	
21	1	W7	DAT	TEST_POINT	

Table 12. Motherboard BOM list (continued)

Item	Quantity	Reference	Part	PCB footprint	Description
22	1	W8	GND	TEST_POINT	
23	1	W9	DAN	TEST_POINT	
24	1	W10	CLK	TEST_POINT	
25	1	W34	Connector_2	Connector_2	
26	1	Y1	4194.304kHz	Auris_hc49ussmd	HC-49/US SMD (Distrelec 335026)

Table 13. Daughterboard BOM list

Item	Quantity	Reference	Part	PCB footprint	Description
1	1	C1	470n	rad_1250x425_ls1075_037	Capacitor X2 12x21x32/11M*470n 275V K
2	1	C2	1n	disc_400x200_ls300x100_037	Capacitor KER X1/Y2 9X5/3M*1.0N 440/330
3	1	C3	22n	sm_0603	
4	1	C4	10n	sm_0603	
5	6	C5,C6,C11,C14	1u	sm_0603	
6	1	C12,C13	100n	sm_0603	
7	4	C7,C8,C9,C10	5n	sm_0603	
8	2	D1,D2	Diode_rele	sm_1812	Diode rectifier SMD*600V 1A
9	2	JP1,JP2	Connector_4x2	jumper_4x2	
10	1	J1	Card_Edge_10	Card_edge_10_mirror	
11	1	L1	220u	sm_1812	Inductor VF82423 1812*220myH 0,1A
12	1	R1	82	rad_725x200_ls300_040	Resistor wire SFR0518 P5 2W*82R K
13	4	R2,R3,R4,R13	150k 1%	sm_0603	
14	2	R5,R12	475 1%	sm_0603	
15	1	R6	3.4 1%	sm_0603	
16	2	R7,R8	1k 1%	sm_0603	
17	1	R9	42.2k 1%	sm_0603	

Table 13. Daughterboard BOM list (continued)

Item	Quantity	Reference	Part	PCB footprint	Description
18	1	R10	2.2M 1%	sm_0603	
19	1	R11	100 1%	sm_0603	
20	2	R14,R17	10	sm_0603	
21	2	R15 or R16,R18	0	sm_0603	
22	1	SH1	170u	r_shunt	
23	1	SH2	170u	r_shunt_2	
24	1	TR1	E4622_X503	VAC_e4622_x503	
25	1	U1	STPMS1	mcs_manual_mlp3x3_16_05_pad	
26	1	V1	460V	disc_450x200_ls300x100_037	Varistor MOKS K10*300V
27	1	W1	N	TEST_POINT	
28	1	W2	F	TEST_POINT	
29	1	W3	DAR	TEST_POINT	
30	1	W4	VREG	TEST_POINT	
31	2	W5,W8	VCC	TEST_POINT	
32	1	W6	GND	TEST_POINT	
33	1	W7	CLK	TEST_POINT	

5 Revision history

Table 14. Document revision history

Date	Revision	Changes
28-Apr-2010	1	Initial release.

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